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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,849	07/10/2003	Hayato Nakanishi	116506	9980

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EXAMINER	
MARESCA, JOSEPH ANDREW	
ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,849	NAKANISHI, HAYATO	
	Examiner	Art Unit	
	Joseph Maresca	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear from the claim whether the width of the second wiring line is to be greater than a single one of the wiring lines or the total width of the wiring lines. The examiner refers applicant to claim 5 where similar matter is claimed in a more distinct manner. For the purposes of making prior art rejections, it is interpreted that the width of the second wiring line need only be wider than that of a single one of the first wiring lines.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoki (US Patent No. 6,788,278).

With respect to claim 1, Aoki discloses an electro-optical device (1) comprising a substrate (2), a plurality of first electrodes (pixel electrode, Figure 1, element 111) disposed in an effective region (2a) on the substrate (2), a second electrode (cathode, 12) acting as a common electrode (column 6, lines 51-56) for the plurality of first electrodes (111), and a plurality of electro-optical elements (11, column 7, lines 54-55) each being disposed between (see Figure 3) the second electrode (12) and the corresponding first electrodes (111).

Aoki further discloses first wiring lines (103R, G, B) to apply power-supply voltages to the first electrodes (111), a seconding wiring line (12a), connected to the second electrode (12, see Figure 3), lying between the effective region (2a) and at least one of a plurality of sides of the substrate (2, see Figure 2), and the area of the second wiring line (12a) dispose on the substrate (2) being larger than a total area of parts of the first wiring lines (103R, G, B), the parts being disposed outside the effective region.

While it is not mentioned in the specification of Aoki, Figure 2 of the present invention is remarkably the same as Figure 2 of the prior art. If the applicant is stating the area of the first wiring lines is smaller than that of the second wiring lines in Figure, than the same holds true for Aoki's drawing.

With respect to claim 2, Aoki further discloses the second wiring line (12a) having a portion that has a width larger than a width of the first wiring lines (103G). It is shown in the drawing of Figure 2 that the width of the first wiring line (103G) is smaller than that of the second wiring line. This is the same as the applicants present invention.

With respect to claim 3, Aoki further discloses a width of the entire second wiring line (12a) being larger than a width of the first wiring lines (103G). It is shown in the drawing of Figure 2 that the width of the first wiring line (103G) is smaller than that of the second wiring line. This is the same as the applicants present invention.

With respect to claim 4, Aoki further discloses each of the plurality of electro-optical elements (11) being place between the second electrode (12) and the corresponding first electrodes (111, see Figure 3), and each including corresponding light-emitting layers (11) that emit light when currents are applied between the second electrode (12) and the corresponding first electrodes (111, column 6 lines 57-67).

Aoki further discloses the plurality of electro-optical elements including a plurality of types of elements (column 11, lines 63-66) classified depending on the color of light emitted (column 11, lines 32-37) from the light-emitting layers and the first wiring lines (103R, G, B) being arranged depending on the color of emitted light (see Figure 2).

With respect to claim 5, Aoki further discloses a width of the second wiring line (12a) disposed outside the effective region (outside of 2a in Figure 2) being larger than a width of part of one of the first wiring lines (103R) arranged depending on the type of the electro-optical elements (see Figure 2), the part being disposed outside the effective region, the one being the widest of the first wiring lines.

From the Figure 2 of Aoki, it is seen that the width of the second wiring would be larger than the width of the first wiring lines.

With respect to claim 6, Aoki further disclose the substrate having a dummy region disposed between the effective region and at least one of a plurality of sides of the substrate (see Figure 3) and the first wiring lines (103R, G, B) and the second wiring line (12a) being arranged between the dummy region (2b) and at least one of a plurality of sides of the substrate (2).

With respect to claim 7, Aoki further discloses the second electrode (12) covering at least the effective region (2a) and the dummy region (2b, see Figure 3).

With respect to claim 8, Aoki further discloses a connection between the second wiring line (12a) and the second electrode (12) lying between the effective region (2a) and at least three of a plurality of sides of the substrate (see Figure 3).

It can be seen in Figure 3 that the connection is made through the semiconductor layers to the wiring line on the ends outside the effective region (2a) in a manner similar to what is displayed in the Figure 3 of the present invention.

With respect to claim 9, Aoki further disclose each of the plurality of first electrodes being include in corresponding pixel electrodes in the effective region (111, see Figure 1), and each including a plurality of control lines (101 and 102) to transmit signals to control the pixel electrodes, and a plurality of control lines (101 and 102) being arrange such that each control line and at least one of the first wiring (103) and the second wiring line (12a) do not cross on the substrate (see Figure 3).

With respect to claim 10, Aoki further discloses the control lines (101 and 102) each including corresponding scanning lines (101) to transmit scanning signals to the corresponding pixel electrodes (111), and also each including corresponding data lines (102) to transmit data signal to the corresponding pixel electrodes.

With respect to claim 11, Aoki further discloses the electro-optical element each including corresponding hole-injection/transport layers (110a) and light-emitting layer (110b) being stacked (column 10, lines 49-52).

With respect to claim 12, Aoki further discloses an electronic apparatus (see Figure 13) comprising the electro-optical device according to claim 1 (see rejection of claim 1 above).

With respect to claim 13, Aoki further discloses a wiring substrate (see Figure 3) for electro-optical devices that each include electro-optical elements (11) that are each disposed between a plurality of corresponding first electrodes (111) and a second electrode (12) acting as a common electrode (column 6, lines 52-56) for the first electrodes (111).

Aoki further discloses the wiring substrate comprises a substrate (2), a plurality of first electrodes disposed on the substrate (111, see Figure 3), first wiring lines (103) to apply power-supply voltages to the first electrodes (column 7, lines 19-22), and a second wiring line (12a) connected to the second electrode (12).

Aoki further discloses the second electrode (12) being disposed outside an effective region (see Figures 2 and 3) having the first electrodes (111) therein (see Figure 3), and the area of the second wiring line (12a) disposed on the substrate (2) being larger than the total area of parts of the first wiring lines (103), the parts being disposed outside the effective region (see Figure 2 and 3) on the substrate (2).

While it is not mentioned in the specification of Aoki, Figure 2 of the present invention is remarkably the same as Figure 2 of the prior art. If the applicant is stating the area of the first wiring lines is smaller than that of the second wiring lines in Figure, than the same holds true for Aoki's drawing.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Published Application 2002/0197392 to Endo which teaches an organic electroluminescent display using a similar drawing to Figure 2 of the present application.

US Patent No. 5,923,119 to Hara which teaches an organic electroluminescent display and a common structure.

US Patent No. 6,690,110 to Yamada which teaches an organic electroluminescent display with a single common electrode and an electrode wiring having a larger width than that of other wirings.

US Patent No. 6,825,820 to Yamazaki which teaches an organic electroluminescent display having power-supply wirings and teaches adjusting the widths of those wirings.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Maresca whose telephone number is (571) 272-5517. The examiner can normally be reached on M-TH and alternate Fridays 7:15 am to 4:45 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chanh Nguyen

CHANH NGUYEN
PRIMARY EXAMINER

JAM

J. Maresca
10/26/2005